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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,077	09/14/2000	Bryan R. Martin	8X8S.243PA	1441

40581 7590 03/28/2005

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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,077	MARTIN ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1-18,20-22 and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1,2,4-6,8,9,14-17, and 20 are amended, and new claims 24-28 are added.

2. Claims 1-18, 20-22, and 24-28 are rejected by the same ground and new ground of rejection necessitated by the amendment.

Drawings

3. The drawings (FIG. 2-7, 11, 12) are objected to because **the labels are difficult to read**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-8, 13,14, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm (U.S. 6,449,269) in view of Dean'326 (U.S. 5,303,326).

Regarding claim 1, Edholm discloses, a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques), and a programmable audio processor chip for processing voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip) comprising:

audio processing circuitry (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29,

col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information).

Edholm does not explicitly disclose a chip comprises DSP voice compression device.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, Dean'326 discloses a chip can be designed to include DSP voice compression device (see col. 3, lines 6-20; DSP chip; and abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include DSP on the ASIC, as taught by Dean'326 and well established teaching in art in the system of Edholm, so that it would increase the transfer rate of data and improve the system; see Dean'326 col. 3, line 6 to col. 4, lines 36. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology, which reduce the size of the VoIP telephone by including a DSP on the ASIC.

Regarding claim 2, Edholm discloses the chip is further adapted to convert the voice data between IP audio data and digital audio data (see FIG. 3, Packetizer 334; also see col. 6, line 1-38; note that Packetizer packetizes/converts between the digitized compressed voice signals/data (from DSP) into IP packet/data).

Regarding claim 3, Edholm discloses an analog-digital (A/D) converter (see FIG. 3, A/D 304) adapted to convert the voice data between analog and digital form (see col. 5, line 56 to col.6, line 3).

Regarding claim 4, Edholm discloses the A/D converter is adapted to convert a voice signal captured at a microphone (see FIG. 3, Microphone 302) of a telephony device (see FIG. 3, IP phone 100) employing the programmable audio processor chip (see col. 6, line 5-13).

Regarding claim 5, Edholm discloses a telephony device (see FIG. 3, IP phone 100) that houses the programmable audio processor chip, wherein the A/D converter is adapted to convert digital data into analog form for use at a speaker of the telephony device (see FIG. 3, Speaker 302 and Sound Generator 306; note that a digitized data are transmitted by the controller into a speaker via A/D converter and sound generator in order to reconstruct analog voice signals.)

Regarding claim 6, Edholm discloses wherein IP network stack includes at least one of: a TCP/IP stack and a H.323 stack (col. 12, line 1-12; note that Edholm's IP telephony device/packetizer utilizes TCP/IP scheme of packetizing.)

Regarding claim 7, Edholm discloses wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities

exchange and negotiation (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates/tear down the call after on-hook.)

Regarding claim 8, Edholm discloses sufficient on-chip RAM (see FIG. 3, Memory 332) to run a connection-less thin client call stack (see col. 6, line 16-65; note that packetizer set up connection for a call utilizing the memory) a TCP/IP stack (see col. 12, line 1-11; the controller utilizes memory for TCP/IP for signaling.) and audio compression protocols (see Fig. 4, and col. 8, line 31 to col. 9, line 56; the controller utilizes memory to process digitized compressed voice data and IP packet data.), wherein the programmable audio processor chip is adapted to function without external system memory (see FIG. 3, Memory 332; note that there is only one on-board memory on ASIC and all operations are performed utilizing this memory.)

Regarding Claim 13, Edholm discloses a telephony communications device (see FIG. 3, IP phone 100) adapted to communicate data including voice data, the device comprising:

DSP functions (see FIG. 3, DSP 310) and a programmable audio processor chip having microcontroller functions (see FIG. 3, a combined system of Controller 314, Packetizer 334, Extractor 322, and Memory 332) and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and digital voice data (see col. 6, line 14-39; note that the packetizer latches/transforms/converts digitized voice signals into IP packets), wherein the programmable audio processor chip includes an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322; see col. 6,

line 14-29, col. 7, line 54-67) and a communication stack ((see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332; see col. 8, line 30 to col. 9, line 56);

an audio capture device communicatively linked to the programmable audio processor chip (see FIG. 3, Microphone 302) and adapted to capture voice signal and communicate the captured voice signal to the programmable audio processor chip (see col. 6, line 5-13; the voice signals are captured by the microphone and transmits towards DSP via A/D converter); and

an audio speaker communicatively linked to the programmable audio processor chip (see FIG. 3, Speaker 302) and adapted to generate sound (see FIG. 3, Sound Generator 306) in response to data communicated from the programmable audio processor chip (see col. 5, line 56 to col.6, line 2; a digitized data are transmitted by the controller into a speaker via A/D converter and sound generator in order to reconstruct analog voice signals.)

Edholm does not explicitly disclose a chip comprises DSP voice compression device.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, Dean'326 discloses a chip can be designed to include DSP voice compression device (see col. 3, lines 6-20; DSP chip; and abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include DSP on the ASIC, as taught by Dean'326 and well established teaching in art in the system of Edholm, so that it would increase the transfer rate of data and improve the system; see Dean'326 col. 3, line 6 to col. 4, lines 36. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy

to carry and store, and the only way to meet user demand is by utilizing ASIC technology, which reduce the size of the VoIP telephone by including a DSP on the ASIC.

Regarding claim 14, Edholm discloses a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques.) and audio processing circuitry (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information).

Dean'326 discloses a chip can be designed to include DSP voice compression device (see col. 3, lines 6-20; DSP chip; and abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include DSP on the ASIC, as taught by Dean'326 and well established teaching in art in the system of Edholm, for the same motivation as described above in claim 13.

Regarding claim 24, Edholm discloses wherein IP network stack includes at least one of: a TCP/IP stack and an IP telephony stack (col. 12, line 1-12; note that Edholm's IP telephony device/packetizer utilizes TCP/IP scheme of packetizing, and IP telephony mechanism/stack).

Regarding claim 25, Edholm discloses, a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress/decompress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed/decompressed utilizing H.323 compressing techniques), a programmable audio processor chip for processing telephony voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip) comprising:

a programmable processing layer (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information).

Edholm does not explicitly disclose a chip comprises DSP voice compression device.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, Dean'326 discloses a chip can be designed to include DSP voice compression and decompression device adapted to compress the telephony voice data (see col. 3, lines 6-20; DSP chip; and abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include DSP on the ASIC, as taught by Dean'326 and well established teaching in art in the system of Edholm, so that it would increase the transfer rate of data and improve the system; see Dean'326 col. 3, line 6 to col. 4, lines 36. It also is well known in the art that the user

constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology, which reduce the size of the VoIP telephone by including a DSP on the ASIC.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm in view of Dean'326 as applied to claim 1 above, and further in view of Sugiura (U.S. 4,248,200) and Waggoner (U.S. 6,218,706).

Regarding claim 9, the combined system of Edholm and Dean'326 discloses wherein the chip or ASIC or IC.

Neither Edholm nor Dean'326 explicitly discloses 250 mw. However, Sugiura discloses the total thermal capacity of IC is about 250 mW (see col. 11, lines 1-2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 250 mW, as taught by Sugiura, in the combined system of Edholm and Dean'326, so that it would provide decreased power consumption and heat generation; see Sugiura col. 10, line 62 to col. 11, lines 2.

Neither Edholm, Dean'326 nor Sugiura explicitly disclose 200 MHz. However, Waggoner discloses 200 MHz for use in IC (see col. 10, lines 33-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 200 MHz, as taught by Waggoner, in the combined system of Edholm, Dean'326 and Sugiura so that it would provide electrostatic protection capability; see Waggoner col. 5, line 19-39; col. 10, lines 16-35; it also is well known in the art it constantly demands longer battery life for a battery powered telephony device so that the user can be utilized without re-

charging frequently. In order to extend the battery life and reduce heat, the power dissipation of the ASIC inside the phone must be minimized.

In addition, a chip can be designed to dissipate 250 mW at 200 MHz or any variation as long as it gives the minimum power dissipation for ASIC. By minimizing ASIC's power dissipation, it will produce small amount of heat and/or consume small amount power (i.e. for battery powered mobile/cordless VoIP phones). The art of reducing the battery power consumption for a mobile/cordless phone in order for the user to utilize the phone battery longer without re-charging is also well known in the art of mobile/cordless telephone. Also, it is also well known in the art that ASIC can also operate at 200 MHz with benchmark performance of power dissipation.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm and Dean'326 as applied to claim 1 above, and further in view of Bertin (U.S. 6,097,243).

Regarding claim 10, the combined system of Edholm and Dean'326 discloses the programmable audio processor circuitry as described above in Claim 1.

Neither Edholm nor Dean'326 explicitly discloses wherein the circuitry is in a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity. However, the above-mentioned claimed limitations are taught Bertin'243. In particular, Bertin'243 teaches wherein the circuitry is in a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity (see col. 2, line 54 to col. 3, line 45; note that in order to reduce power consumption the semiconductor device is put into a groggy mode (i.e. power-down mode) by reducing operational clock speed during inactivity).

In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Bertin'243, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a mechanism to reduce the clock speed during inactivity, as taught by Bertin'243. The motivation to combine is to obtain the advantages/benefits taught by Bertin'243 since Bertin'243 states at col. 2, line 54-56 that such modification would make it possible to reduce power consumption while maintaining full functionality of the semiconductor device.

8. Claim 11, 26-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm and Dean'326 as applied to claims 1 and 25 above, and further in view of Mason (U.S. 6,272,451).

Regarding claim 11, the combined system of Edholm and Dean'326 discloses the programmable audio processor circuitry as described above in Claim 1.

Neither Edholm nor Dean'326 explicitly discloses wherein the circuitry is adapted to be programmed using C programming language. However, the above-mentioned claimed limitations are taught Mason'451. In particular, Mason'451 teaches wherein the circuitry is adapted to be programmed using C programming language (see col. 9, line 19-29; note that FPGA microcontroller designs are usually done in the C-language). In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Mason'451, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a mechanism to

program the circuitry/chip with C-programming language, as taught by Mason'451. The motivation to combine is to obtain the advantages/benefits taught by Mason'451 since Mason'451 states at col. 4, line 66 to col. 5, line 10 that such modification would make it possible to allow programmable logic users to design, with ease, FPSLIC devices which contain microprocessors by utilizing software tool.

Regarding Claim 26, the claim, which has substantially disclose all the limitations of the respective claim 11. Therefore, it is subjected to the same rejection.

Regarding claim 27, Mason'451 teaches wherein the circuitry is adapted to be programmed using assembly language (see col. 9, line 19-29; note that FPGA microcontroller designs are usually done in the C-language or assembly language). In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Mason'451, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a mechanism to program the circuitry/chip with assembly language, as taught by Mason'451. The motivation to combine is to obtain the advantages/benefits taught by Mason'451 since Mason'451 states at col. 4, line 66 to col. 5, line 10 that such modification would make it possible to allow programmable logic users to design, with ease, FPSLIC devices which contain microprocessors by utilizing software tool.

Regarding claim 28, the combined system of Edholm and Dean'326 discloses the DSP voice compression and decompression device is an executable function on the programmable audio process chip as described above in Claim 25.

Neither Edholm nor Dean'326 explicitly discloses assembly language. However, the above-mentioned claimed limitations are taught Mason'451. In particular, Mason'451 teaches wherein the circuitry is adapted to be programmed using assembly language (see col. 9, line 19-29; note that FPGA microcontroller designs are usually done in the C-language assembly language). In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Mason'451, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a mechanism to program the circuitry/chip with assembly language, as taught by Mason'451. The motivation to combine is to obtain the advantages/benefits taught by Mason'451 since Mason'451 states at col. 4, line 66 to col. 5, line 10 that such modification would make it possible to allow programmable logic users to design, with ease, FPSLIC devices which contain microprocessors by utilizing software tool.

9. Claim 12 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm and Dean'326 as applied to claim 1 and 13 above, and further in view of Maeda (U.S. 5,884,074).

Regarding claim 12, the combined system of Edholm and Dean'326 discloses telecommunication device comprising the programmable audio processor circuitry as described above in Claim 1. Furthermore, Edholm discloses a CPU (see FIG. 3, Controller) and execution space with memory on the chip (see col. 6, line 16-65; col. 12, line 1-11; Fig. 4, and col. 8, line 31 to col. 9, line 56; note that the controller executes memory for packetizing, TCP/IP for signaling, and processing of digitized voice.)

Neither Edholm nor Dean'326 explicitly discloses the flash-style, non-volatile memory, that includes embedded firmware for that device and wherein the circuitry of the Flash-cache architecture adapted to enable a CPU to boot and run code from an external Flash-style device, and mix this execution space with memory. However, the above-mentioned claimed limitations are taught Maeda'074. In particular, Maeda'074 teaches the flash-style, non-volatile memory (see FIG. 1, Flash Memory 11), that includes embedded firmware for that device and wherein the circuitry of Flash-cache architecture adapted to enable a CPU (see FIG. 1, CPU 17) to boot and run code from an external Flash-style device (see FIG. 1, Flash Memory 11; note that CPU executes the boot program stored in the boot program area of the flash memory), and mix this execution space with memory (see FIG. 1, RAM 2; see col. 1, line 20 to col. 2, line 22; note that CPU stores programs in the RAM. Thus, it is clear that combined memories from both memory units (i.e. Flash and RAM) must be utilized for CPU execution).

In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Maeda'074, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a microcomputer/chip which has a mechanism to execute user boot programs from the flash memory and store the programs into RAM, as taught by Maeda'074. The motivation to combine is to obtain the advantages/benefits taught by Maeda'074 since Maeda'074 states at col. 1, line 64-66 that such modification would make it possible to provide a microcomputer/chip capable of releasing the entire area of the flash memory for a user program area.

Regarding claim 15, the combined system of Edholm and Dean'326 discloses telecommunication device comprising the programmable audio processor circuitry as described above in Claim 13. Furthermore, Edholm discloses a CPU (see FIG. 3, Controller) and execution space with internal memory on the programmable audio processor chip (see col. 6, line 16-65; col. 12, line 1-11; Fig. 4, and col. 8, line 31 to col. 9, line 56; note that the controller executes memory for packetizing, TCP/IP for signaling, and processing of digitized voice.)

Neither Edholm nor Dean'326 explicitly discloses the flash-style, non-volatile memory, that includes embedded firmware for that device and wherein the circuitry of the Flash-cache architecture adapted to enable a CPU to boot and run code from the Flash-style non-volatile, and mix this execution space with memory. However, the above-mentioned claimed limitations are taught Maeda'074. In particular, Maeda'074 teaches the flash-style, non-volatile memory (see FIG. 1, Flash Memory 11), that includes embedded firmware for that device and wherein the circuitry of Flash-cache architecture adapted to enable a CPU (see FIG. 1, CPU 17) to boot and run code from an external Flash-style device (see FIG. 1, Flash Memory 11; note that CPU executes the boot program stored in the boot program area of the flash memory), and mix this execution space with memory (see FIG. 1, RAM 2; see col. 1, line 20 to col. 2, line 22; note that CPU stores programs in the RAM. Thus, it is clear that combined memories from both memory units (i.e. Flash and RAM) must be utilized for CPU execution).

In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Maeda'074, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to modify the combined system of Edholm and Dean'326, by providing a microcomputer/chip which has a mechanism to execute user boot programs from the flash memory and store the programs into RAM, as taught by Maeda'074. The motivation to combine is to obtain the advantages/benefits taught by Maeda'074 since Maeda'074 states at col. 1, line 64-66 that such modification would make it possible to provide a microcomputer/chip capable of releasing the entire area of the flash memory for a user program area.

Regarding claim 16, the combined system of Edholm, Dean'326 and Maeda'074 discloses the telephony communications device, further comprising a plurality of communications stacks, DSP codes, RAM and external flash memory as described above in Claims 13 and 15. Furthermore, Edholm teaches the device (see FIG. 3, Controller) adapted to run compute-intensive DSP code out of the internal memory and to run the communication stacks out of memory (see col. 6, line 16-65; col. 12, line 1-11; Fig. 4, and col. 8, line 31 to col. 9, line 56; note that the controller executes memory for processing of digitized voice (i.e. running DSP code), packetizing and TCP/IP for signaling (i.e. running communication stacks)). In addition Maeda'074 discloses the device (see FIG. 1, CPU 17) is adapted to run programs/instructions/tasks from an external flash memory as described above in Claim 15.

Neither Edholm, Dean'326, nor Maeda'074 explicitly discloses the device is adapted to run the communication stacks out of flash-style, non-volatile memory. However, the above-mentioned claimed limitations are well known in the art. In particular, the device can be adapted to run compute-intensive DSP code out of internal memory and to run the communication stacks out of flash-style, non-volatile memory. Edholm teaches a device

which all computations and processes will be utilized/run by the single memory. Maeda'074 also teaches utilizing the flash memory to run/boot the user-defined programs and RAM to store programs. Thus, it is obvious and well known in the art that the computational functions and processes can be divided/distributed between various type memories (i.e. RAM vs. ROM/Flash-memory) in any computer related device. Thus, Flash memory can be used to boot and run the programs to set up the TCP/IP communication, and RAM memory can be used to store programs for DSP and packetizing devices.

In view of this, having the combined system of Edholm, Dean'326 and Maeda'074, then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm, Dean'326 and Maeda'074, by assigning specific function for each type of memories. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to avoid process overloading in computer related device by assigning the computational and processing load among memory units.

Regarding claim 17, Edholm teaches the device is adapted to run the compute-intensive DSP code including at least one of: audio codecs, acoustic echo cancellation and framing (see col. 6, line 1-12; note that DSP encode and decode the digitized voice by using echo cancellation procedures.)

Regarding claim 18, Edholm discloses wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation (see col. 8, line 30 to col. 9, line 56; not that the controller

instructs/processes the packetizer to establish call connection setup and terminates/tear down the call after on-hook.)

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm in view of Dean'326, and further in view of Dean (U.S. 5,553,276).

Regarding Claim 20, Edholm discloses an IP telephony communications network (see FIG. 1, IP telephony network) comprising:

a plurality of IP telephony devices (see FIG. 1, plurality of IP phones 100 and 171) each having a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques.), and a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques.); a programmable audio processor chip for processing voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip.) comprising:

audio processing circuitry (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information);

a CPU (see FIG. 1, Phone Server 110) adapted to communicate with the plurality of IP telephony communications devices (see FIG. 1, IP telephone 100 and a combined IP telephone comprises computer 170 with speaker 171 and microphone 172) and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols (see col. 4, lines 30-55; and col. 8, line 30 to col. 9, line 55; note that phone server programs/instructs/commands the IP phones regarding call/connection), the CPU adapted to execute a plurality of instructions simultaneously (see col. 4, lines 30-55; the server executes the instructions simultaneously);

a communications link (see FIG. 1, links in the network 130) coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including

voice IP data (also see col. 4, line 21 to col. 5, line 9; note that VoIP data are transmitted/received to/from the other VoIP phones and phone server 110 via the network.)

Edholm does not explicitly disclose a chip comprises DSP voice compression device. However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, Dean'326 discloses a chip can be designed to include DSP voice compression device (see col. 3, lines 6-20; DSP chip; and abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include DSP on the ASIC, as taught by Dean'326 and well established teaching in art in the system of Edholm, so that it would increase the transfer rate of data and improve the system; see Dean'326 col. 3, line 6 to col. 4, lines 36. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology, which reduce the size of the VoIP telephone by including a DSP on the ASIC.

Neither Edholm nor Dean'326 explicitly discloses a standard RISC 5-stage pipeline. However, the above-mentioned claimed limitations are well known in the art of integrated circuitry. In particular, Dean'276 discloses CPU/processor having a standard RISC 5-stage pipeline (see FIG. 1, CPU/processor with a Standard RISC 5-stage pipeline; see col. 8, lines 30-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use standard RISC 5-stage pipeline, as taught by Dean'276 and well established teaching in art in the combined system of Edholm and Dean'326, so that it would reduce average number of cycles, thereby significantly improve processor performance; see Dean'276 col. 8, line 15-, lines 36. It also is well known in the art that the

user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology. Moreover, by designing the standardized CPU, it will enable to inter-operate with the other CPU or devices.

11. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm and Dean'326 as applied to claim 20 above, and further in view of Adelman (U.S. 5,598,362).

Regarding claim 21, the combined system of Edholm and Dean'326 discloses the CPU as described above in Claim 20.

Neither Edholm nor Dean'326 explicitly discloses wherein the CPU further comprises a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU). However, the above-mentioned claimed limitations are taught by Adelman'362. In particular, Adelman'362 teaches a DSP Multiply Accumulate (DSPMAC) unit (see FIG. 2, Multiplier 76 of Data Arithmetic Logic unit performing DSP multiply/accumulate (MAC) operation; see col. 1, line 29-34) and an Address Generation Unit (AGU) (see FIG. 1, Address Generation Unit 36, AGU; see col. 4, line 6-14). In view of this, having the combined system of Edholm and Dean'326, then given the teaching of Adelman'362, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and Dean'326, by providing DSP MAC and AGU units, as taught by Adelman'362. The motivation to combine is to obtain the advantages/benefits taught by Adelman'362 since Adelman'362 states at col. 1, line 45 to col.1, line 30-55 that such modification would make it possible to provide greater voice accuracy.

Regarding claim 22, the combined system of Edholm, Adelman'362, and Dean'326 discloses the AGU and CPU as described above in Claims 20 and 21. In particular, Edholm teaches the controller which performs the function of the CPU. Adelman'362 teaches AGU, which generates the address of the instruction (see col. 4, line 6-54). Also, it is well known in the art that the function of a controller/CPU is to execute instructions/tasks by calculating the address of the operand.

Neither Edholm, Dean'326 nor Adelman'362 explicitly discloses wherein the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU. However, the above-mentioned claimed limitations are taught by well known in the art. In particular, the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU. Note that both AGU and controller/CPU have the functionality of generating/calculating the addresses, and they are both in the same ASIC chip. Thus, it is clear that they both must calculate/generate the address in parallel manner. In view of this, having the combined system of Edholm and Adelman'362, then given the well-established teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm and well-established teaching in the art, by providing a mechanism for the controller/CPU and AGU units which perform the address calculation/generation in parallel manner as taught by well-established teaching in the art. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art since such modification would make it possible to provide faster CPU/controller processing since the tasks are now performed in parallel manner.

Allowable Subject Matter

12. Claim 23 is allowed.

Response to Arguments

13. Applicant's arguments filed 1-18-2005 have been fully considered but they are not persuasive.

Regarding claims 1-18 are 20-22, and 24-28, the applicant argued that, "...the Edholm does not teach a chip with either an IP network stack or a communication stack, **which each include a protocol layer higher than the IP layer**...Edholm does not includes **any layers higher than the IP layer**..." in page 9, paragraph 3.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **each (i.e. IP network stack and communication stack) include a protocol layer higher than the IP layer or any layers higher than the IP layer)** are **not** recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding claims 1-18 are 20-22, and 24-28, the applicant argued that, "...Edholm reference teaches or suggests the limitations directed to a programmable audio processor chip for processing voice data that includes an IP network stack and/or a

communication stack...the Edholm does not teach a chip with either an IP network stack or a communication stack..." in page 9, paragraph 3.

In response to applicant's argument, the examiner respectfully disagrees that Edholm reference teaches or suggests the limitations directed to a programmable audio processor chip for processing voice data that includes an IP network stack and/or a communication stack...the Edholm does not teach a chip with either an IP network stack or a communication stack.

Edholm discloses an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network which are received from the network); and a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information). Edholm also teaches a programmable audio processor chip for processing voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components

within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip).

The applicant argued that, "...col. 12, line 1-12 of the Edholm clearly stated that higher OSI layer (layer 4+) signaling (e.g. TCP/IP and/or H.323) are processed by a separated phone server operating in tandem with the IP telephone... Edholm clearly does not include any layers higher than the IP layer, and thus does not include an IP network stack, which includes a protocol layer higher than the IP layer..." in page 9, paragraph 3.

In response to applicant's argument, the examiner respectfully disagrees that col. 12, line 1-12 of the Edholm clearly stated that higher OSI layer (layer 4+) signaling (e.g. TCP/IP and/or H.323) are processed by a separated phone server operating in tandem with the IP telephone... Edholm clearly does not include any layers higher than the IP layer, and thus does not include an IP network stack, which includes a protocol layer higher than the IP layer.

Note that "each (i.e. IP network stack and communication stack) include a protocol layer higher than the IP layer or any layers higher than the IP layer" not being claimed (see above response) as recited in above response. In addition, col. 12, line 1-12 of Edholm clearly states follows:

"...the controller 314 transitions to state 558 in which the ***controller 314*** *directs that the* ***packetizer 334 develop appropriate layer 4 + overhead (such as TCP/IP packet sequencing number)*** *in a routine manner. Thereafter, the controller transitions to state 554 where it directs that packetizer 334 and checksum generator 336 to* ***create and deliver*** *a*

complete layer 4+ packet to the MAC 328 for transmission across the network 130 *to the other telephony device(s) engaged in a layer 4+ call or session with the telephone 600...*"

For the above cited paragraph of Edholm, it is clear that controller 314, which is within of audio processor chip device of the IP telephone (see FIG. 3), instructing packetizer 334, which is within audio processor chip device of the IP telephone (see FIG. 3), creating and delivering layer 4+ packet to the network, and this process, performs by the controller 314 and packetizer 334, is clearly not performed by the a separate phone server as applicant argued above.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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